



REVCO PRODUCTS

ELECTRONIC CONTRACT MANUFACTURER
PCB LAYOUT • ASSEMBLY • TEST

TECHNICAL PAPER



TEN DFM CHECKS THAT CUT PCB ASSEMBLY COST BEFORE YOU QUOTE

A Design for Manufacturability field guide across the manufacturing value chain, from bare board through box build.

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ABSTRACT

The cost of an assembly is largely committed the moment the design data package leaves engineering, long before the first quote is returned. Ambiguous fabrication notes, nonstandard land patterns, unbalanced thermal pads, and components selected without regard to sourcing risk all introduce costs that may be invisible on the schematic.

This paper presents ten DFM checks that can reduce PCB assembly costs across the manufacturing value chain, from bare board fabrication and SMT/THT assembly to mixed-technology processing, test, and system integration. Each check identifies a common failure mode, explains how it drives cost, and highlights changes that can be made early in the design cycle, when fixes are easiest and least expensive.

Written for both design engineers and sourcing professionals, the paper provides a common framework for addressing design, component selection, and supply-chain decisions that can accelerate quoting, reduce respins, improve first-pass yield, and lower total cost throughout the life of the program.

DFM IS A COST DECISION, NOT A COMPLIANCE STEP

Design for Manufacturability (DFM) is the practice of designing a product so it can be manufactured reliably, repeatably, and cost-effectively. It is not simply a review performed by a fabricator or electronics manufacturing services (EMS) provider after the design is complete. Effective DFM begins during design, when decisions about board geometry, component selection, land patterns, materials, tolerances, test access, and assembly processes can still be changed at minimal cost.

This distinction matters because DFM decisions directly influence manufacturing cost, yield, quality, and schedule. The objective is to identify and eliminate unnecessary cost drivers before they become embedded in the product and production process.

The value of DFM increases the earlier it is applied. A problem identified in CAD may require only minutes of engineering time to correct. The same problem discovered during fabrication can trigger engineering questions, data revisions, re-quotes, and schedule delays. At assembly, it can require tooling changes, process adjustments, rework, or scrap. In the field, corrective action can include product returns, replacements, and other warranty costs.

THE DATA PACKAGE: THE CHECK BEFORE THE CHECKS

A complete, well-defined data package provides the foundation for DFM analysis, accurate quoting, and manufacturing readiness. An incomplete or ambiguous package introduces cost before a board is built. Missing fabrication requirements, unclear performance criteria, absent test data, conflicting revisions, or files requiring interpretation can prevent a manufacturer from confidently defining scope and cost.

At minimum, the package should clearly define applicable workmanship and performance requirements, fabrication and assembly requirements, stackup, controlled impedances, surface finish, and other critical specifications. It should also include the data needed for bare-board electrical testing, such as a netlist, along with complete fabrication outputs. Intelligent formats such as IPC-2581 or ODB++ can consolidate design and manufacturing data into a more integrated dataset, reducing the manual reconciliation required when information is distributed across separate Gerber, drill, netlists, drawings, and other files.

Time invested in a complete, standards-compliant data handoff can prevent days of downstream clarification and delay. For sourcing teams, data-package completeness should be treated as a requirement for accurate, comparable quotes, not an administrative detail.

THE TEN CHECKS

The ten checks follow the manufacturing value chain, from bare board through box build, with a final check on component and BOM health that affects every stage. Each identifies what to evaluate, the risk if overlooked, and the cost lever it influences. They require disciplined attention early in the design cycle, when changes are easiest and less expensive to make.

Bare-Board Fabrication

Check 1 — Annular Ring, Drill Size, Aspect Ratio & Mask Geometry

This check evaluates the drilled and imaged features of the bare PCB, including annular rings, drill sizes, hole aspect ratios, solder mask dams, silkscreen clearance and legibility, and surface finish.

Drill wander and layer-to-layer misregistration reduce the effective annular ring. When the design provides insufficient margin, normal fabrication variation can produce tangent or broken annular rings that may violate IPC-A-600 or IPC-6012 acceptance requirements. High-aspect-ratio holes also make uniform copper plating more difficult, raising the risk of barrel plating defects that can compromise interconnect reliability during thermal cycling and field operation.

Solder mask and silkscreen deserve similar scrutiny. Mask dams that are too narrow for the fabricator's process may not resolve reliably, increasing the risk of solder bridging between closely spaced fine-pitch pads. Silkscreen overlapping exposed pads can interfere with solderability, while missing or illegible reference designators can slow inspection, troubleshooting, and rework.

Surface finish should also be reviewed against component and assembly requirements. ENIG's flat surface makes it well suited to fine-pitch and area-array components, while HASL can introduce greater surface-height variation. For consigned boards using HASL, any potential impact on paste printing, component placement, or solder-joint consistency should be identified and discussed with the customer before assembly.

Cost Lever Adequate annular ring and manufacturable aspect ratios improve fabrication yield and reduce interconnect reliability risk. Using the fabricator's standard drill sizes can avoid unnecessary custom tooling charges, while manufacturable mask geometry reduces fine-pitch bridging and rework. Because these limits are process-dependent, drill, annular-ring, aspect-ratio, and mask requirements should be verified against the fabricator's capability specifications rather than generic design rules.

Annular ring and drill registration

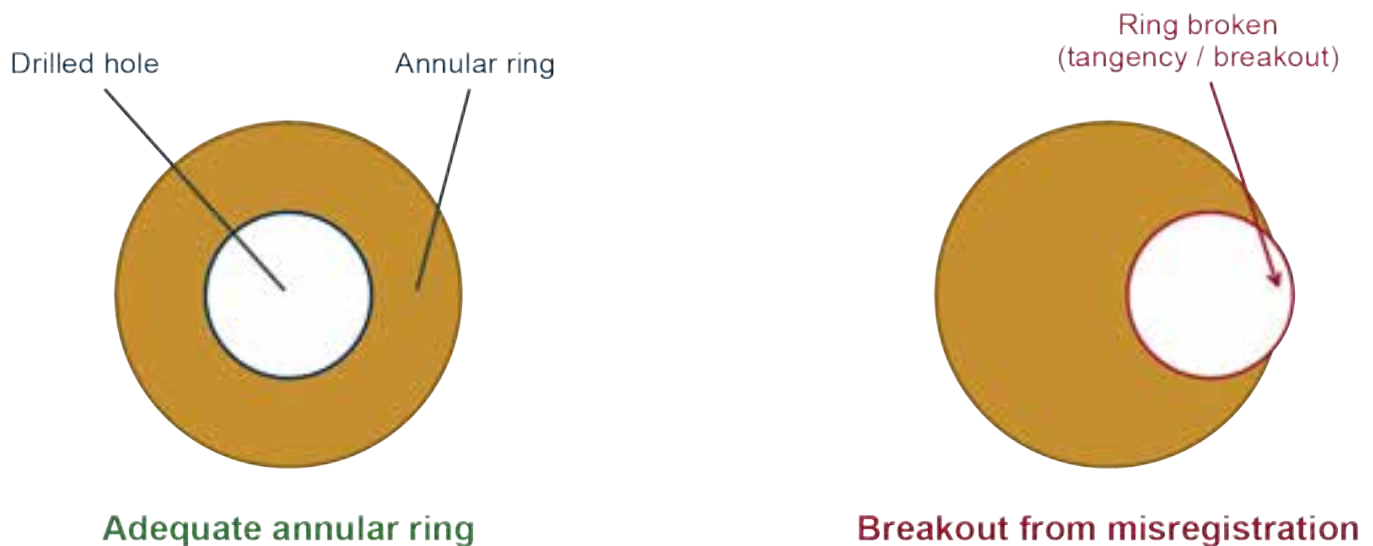


Figure 1. Annular ring and drill registration
Original diagram. 360Circuits for Revco Products.

Check 2 — Panelization, Tooling Rails, Fiducials & Edge Clearance

This check reviews array layout, tooling rails and holes, global fiducial placement, component clearance from board edges, and the selected depanelization method, such as breakaway tabs or V-scoring.

Components placed too close to routed edges, breakaway tabs, or V-scores can be subjected to excessive mechanical stress during depanelization, potentially cracking components, solder joints, or the PCB itself. Clearance requirements should therefore account for both component type and the intended depanelization process.

Boards supplied without adequate tooling rails, fiducials, or tooling holes may require custom carriers or additional manual handling. Both add cost: carriers introduce nonrecurring tooling expenses, while manual handling reduces throughput, limits automation, and increases process variability.

Panel dimensions and features must also be compatible with the assembly line's conveyor, handling, and depanelization equipment. Poor panel design can reduce the number of boards processed per cycle, complicate automated handling, increase material waste, and add unnecessary manufacturing costs.

Cost Lever Panelization designed around the assembly process improves throughput, supports automated handling, and can eliminate custom carrier tooling. Properly positioned fiducials support reliable machine alignment and placement accuracy, while appropriate board-edge clearance reduces depanelization damage and rework. Optimizing the panel for the line it will run on can reduce both recurring assembly costs and non-recurring tooling expenses.

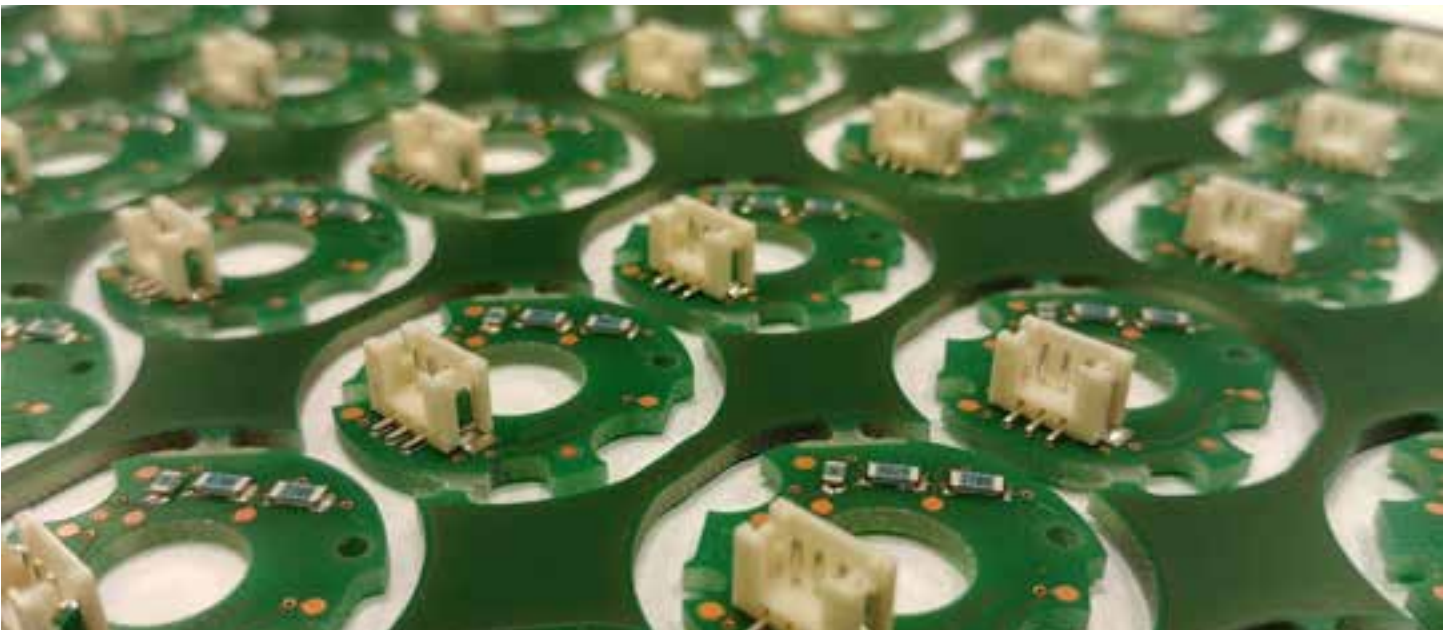


Figure 2. Panelized array with tooling rails and fiducials

A PCB delivered as a panel or array, showing multiple boards, break-away framing, and the tooling border that lets the line run the job fully automated.

Surface Mount Assembly

Check 3 — Land-Pattern Accuracy to IPC-7351

The land pattern defines the physical connection between a surface mount component and the PCB. Errors in pad geometry can compromise assembly yield and solder-joint reliability. This check verifies that each surface mount land pattern follows IPC-7351 guidance, component manufacturer recommendations, and assembly requirements, including appropriate toe, heel, and side fillet allowance. It also confirms that the selected density level provides the appropriate balance among component spacing, manufacturability, and reliability.

Incorrect or poorly interpreted footprints can result in multiple failure modes. Undersized or misaligned pads can produce weak or open solder joints, while oversized or improperly spaced pads can increase the risk of solder bridging or poor component alignment. When footprint errors are not identified early, they may not become apparent until first-article assembly, resulting in costly board revisions, scrapped components, rework, and schedule delays.

Component availability should also be considered during footprint review. Where practical, combination footprints that support electrically compatible alternate packages or component options can allow production to continue when the preferred part is unavailable. Each alternative must be reviewed for pad geometry, spacing, polarity, electrical compatibility, thermal performance, and assembly requirements. Properly designed alternate footprints can prevent a supply-chain issue from forcing an otherwise unnecessary PCB respin.

Cost Lever Validated land patterns improve first-pass yield and reduce the risk of rework and PCB respins. Correct pad geometry promotes component self-alignment during reflow, while a controlled, standardized footprint library helps prevent recurring design errors. Together, these practices eliminate a significant source of avoidable assembly cost and schedule disruption.

IPC-7351 land pattern: fillet and courtyard geometry

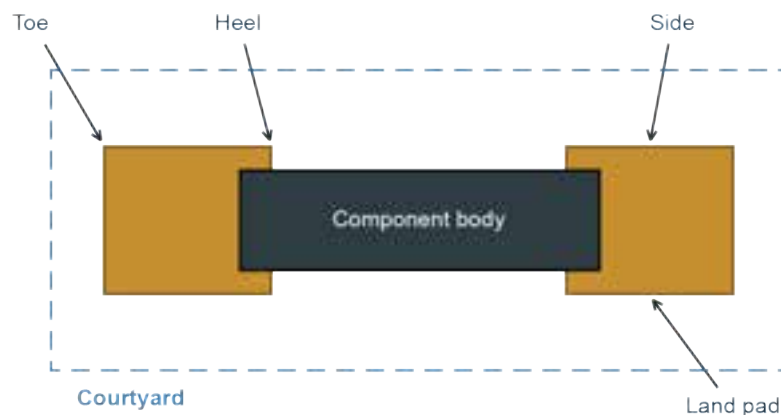


Figure 3. IPC-7351 land pattern: fillet and courtyard geometry
Original diagram. 360Circuits for Revco Products.

Check 4 — Courtyards, Component Spacing & Placement Orientation

This check evaluates component placement and spacing across the PCB, including IPC-7351 courtyards, body-to-body clearance, component orientation, and keep-out areas around connectors and other mechanically constrained components.

Adequate spacing is required for pick-and-place nozzles, inspection equipment, and rework tools. Components placed too close together can interfere with automated placement, restrict rework access, and increase the risk of solder bridging between adjacent leads or pads.

Component height also matters. Tall or high-thermal-mass components placed near smaller parts can create localized thermal effects during reflow and may obstruct shorter components during automated optical inspection. Appropriate clearance between components of different heights supports reflow consistency, inspection coverage, and rework access.

Consistent orientation simplifies placement programming and inspection. Where practical, polarized components and similar package types should use consistent orientation throughout the design. This reduces programming complexity and makes visual inspection easier.

Component distribution between the two sides of the PCB can also significantly affect assembly cost. A board with most surface mount components on one side and only a few on the second side still requires a second placement and reflow cycle. When board space, electrical performance, and thermal requirements permit, consolidating surface mount components on one side can eliminate these extra process steps, reduce handling, and improve throughput.

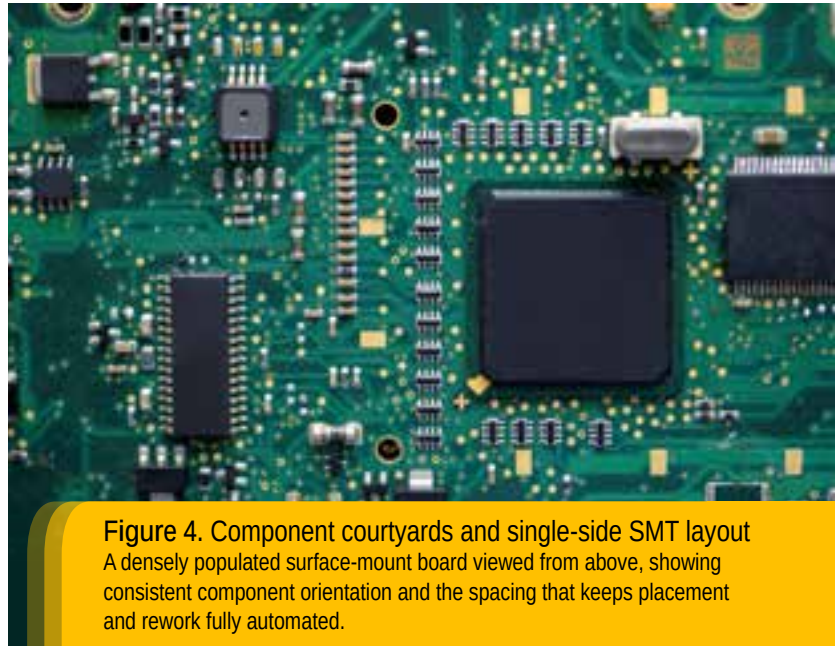


Figure 4. Component courtyards and single-side SMT layout
A densely populated surface-mount board viewed from above, showing consistent component orientation and the spacing that keeps placement and rework fully automated.

Cost Lever Proper courtyards and component spacing support automated placement, reduce bridging and rework, and preserve access for rework and repair. Consistent orientation speeds programming and inspection, while one-sided assembly, where practical, can eliminate an entire placement and reflow cycle. These improvements reduce cycle time and rework costs, with the benefits compounding on high-component-count boards.

Check 5 — Thermal Balance & Thermal Relief

Small, two-terminal passive components are often among the most numerous parts on a PCB, making their reflow behavior an important contributor to overall assembly yield.

This check evaluates pad symmetry and thermal balance between component terminations, particularly where one pad connects to a large copper plane or pour. It also verifies the appropriate use of thermal-relief connections to reduce excessive heat sinking.

When one pad is connected directly to a large copper area, it can heat more slowly than the opposite pad. If the two solder joints reach reflow at different times, unequal wetting and surface-tension forces can lift one end of the component, producing a tombstone defect. Thermal imbalance can also contribute to incomplete or inconsistent solder joints.

Because resistors and capacitors often appear in large quantities, even a low defect rate can significantly reduce first-pass yield. Balanced copper connections, consistent pad geometry, and appropriate thermal reliefs help both terminations reflow more uniformly, improving solder-joint consistency and assembly yield.

Cost Lever Proper thermal relief and end-to-end symmetry improve first-pass yield across some of the highest-volume components on the board, reducing tombstoning and associated rework. Addressing thermal imbalance during layout adds little or no production cost and prevents a defect mechanism that can otherwise recur across every unit assembled.

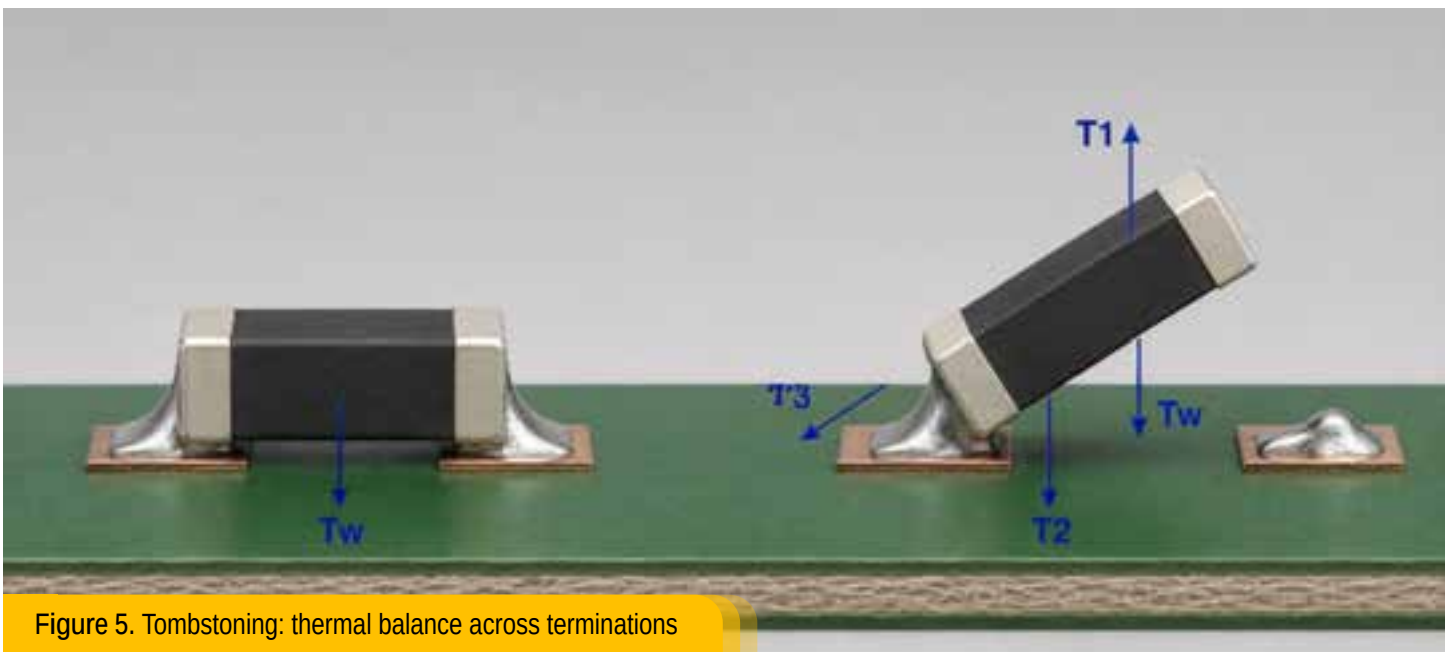


Figure 5. Tombstoning: thermal balance across terminations

Check 6 — Stencil & Paste Aperture Design

Consistent solder paste deposition is critical to achieving reliable joints on the first reflow pass. This check evaluates stencil thickness and aperture size, shape, and location in accordance with IPC-7525 standards. It also evaluates aperture area ratio and aspect ratio, which influence solder paste transfer and release from the stencil to the pad.

Apertures that are too small or have an unfavorable area ratio may retain paste in the stencil, resulting in insufficient solder deposits, poorly formed joints, or opens. Oversized apertures can deposit excessive paste, increasing the risk of bridging, solder balling, and component movement. Specialized aperture geometries, such as home-plate designs, can be used where needed to control paste volume and improve print performance for specific component or process requirements.

For QFN and other bottom-terminated components, the large exposed-pad aperture is typically divided into smaller windowpane openings. This controls total paste volume and provides pathways for flux volatiles to escape during reflow. A single large opening can deposit excessive paste, trap volatiles, contribute to voiding, and cause the component to float or tilt. BGA aperture design also requires careful control to achieve consistent paste deposits across the array, minimizing bridging risk.

Cost Lever Disciplined stencil and aperture design improves first-pass yield by reducing insufficient solder, opens, bridging, and other paste-related defects. Controlling paste volume at the stencil prevents recurring defects before they reach AOI, X-ray inspection, or rework, reducing inspection burden, repair time, and overall assembly cost.



Figure 6. Stencil printing and paste deposition

A solder paste printer laying paste through a stencil onto the board, the step that sets deposit volume before placement and reflow.

Through-Hole & Mixed Technology

Check 7 — Through-Hole Process Compatibility & Pin-in-Paste (PiP)

Through-hole components add insertion and soldering operations, so each should serve a necessary function and be designed for a defined assembly process. This check verifies finished hole size relative to lead dimensions, appropriate thermal relief for pads connected to large copper areas, component orientation for wave soldering, and compatibility with the intended soldering method. It also determines whether components are best suited for pin-in-paste (PiP) reflow, selective soldering, wave soldering, or hand soldering.

Holes that are too small can prevent automated insertion or damage leads, while oversized holes can make it difficult to achieve consistent barrel fill. Pads connected directly to large copper planes can draw heat away from the joint, resulting in poor wetting, insufficient solder fill, or open connections. For wave soldering, component placement and orientation should also minimize solder shadowing and bridging.

Where appropriate, PiP can integrate through-hole components into the SMT reflow process, eliminating a separate soldering operation. Successful PiP requires sufficient solder paste volume, components capable of withstanding the reflow thermal profile, and appropriate hole, lead, pad, and stencil geometry.

Cost Lever Designing through-hole parts for pin-in-paste (PiP) can eliminate a secondary soldering operation, allowing them to be processed in the same reflow cycle as surface mount components, a significant labor and cycle-time saving on mixed-technology assemblies. Where PiP is not practical, designing specifically for selective or wave soldering helps preserve automation and minimize hand soldering. Reducing unnecessary through-hole components can further lower drilling and assembly costs, frees inner-layer routing area, and simplifies manufacturing.

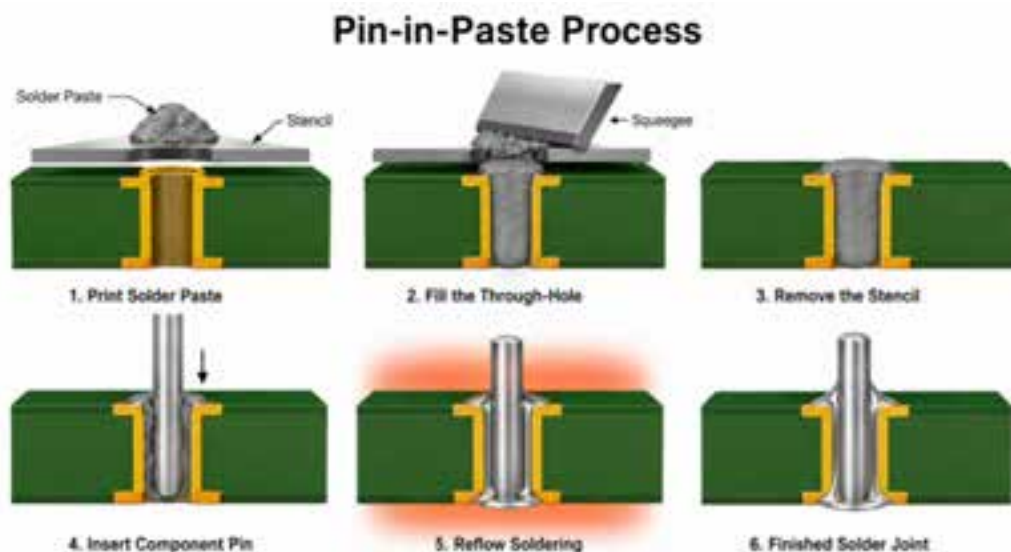


Figure 7. Pin-in-paste: through-hole reflowed on the SMT line

Test and Inspection

Check 8 — Designing for Testing & Automated Optical Inspection (AOI)

Effective test and inspection coverage must be designed into the product. This check verifies access for in-circuit testing (ICT), including properly sized and spaced test pads, preferably accessible from one side of the assembly. It also evaluates provisions for functional testing and, where supported by the components and architecture, JTAG/boundary-scan access to otherwise difficult-to-test circuit nodes and interconnects.

Global and local fiducials are reviewed to support accurate automated optical inspection (AOI) and other vision-based processes. Properly positioned fiducials provide reliable reference points for board alignment and inspection of fine-pitch and high-density areas. Missing or poorly positioned fiducials can reduce inspection effectiveness or require additional setup.

Test strategy should be considered early enough to influence PCB layout. Inadequate probe access can reduce fault coverage, require more complex test fixtures, or force reliance on slower manual methods. Functional test interfaces should provide practical access to power, signals, communications, and other functions needed to verify assembled-board performance.

Bare-board electrical test should also be supported with complete design data, including an IPC-D-356 netlist where applicable. This allows the fabricator to identify opens and shorts before components and assembly cost are added to the board.

Design for test: bed-of-nails access to test points

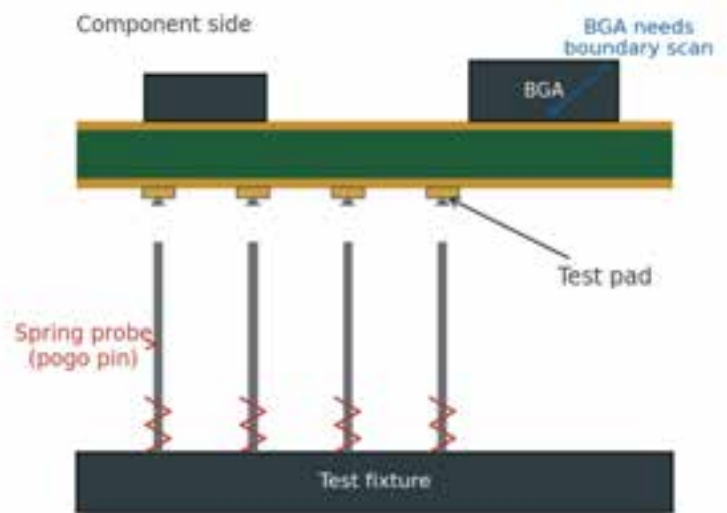


Figure 8. Design for test: bed-of-nails access to test points

Cost Lever Designing for test and inspection moves defect detection earlier in the manufacturing process, when failures are generally less costly to correct. Accessible test points and well-planned interfaces simplify fixtures and reduce manual testing, while properly positioned fiducials support efficient automated inspection. Bare-board electrical test catches opens and shorts before assembly value is added, reducing rework and the risk of defects escaping to the customer.

Box Build and System Integration

Check 9 — Connector Access, Keying & Harness Routing

Manual assembly time is a significant driver of box-build cost, making efficient system integration an important DFM consideration. This check verifies connector location and orientation, harness lengths and routing, tool access for fasteners and standoffs, and poka-yoke (mistake proofing) features that simplify assembly and prevent connection errors.

Keyed and polarized connectors should be used where practical to prevent incorrect mating or reversed connections. Clear, consistent connector and cable identification provides another layer of error prevention. Poorly positioned or ambiguous connectors slow assembly and increase the risk of wiring errors.

Tool access should also be considered during mechanical layout. Fasteners and standoffs should be positioned so operators can reach them with the intended tools without removing unrelated components or requiring awkward assembly sequences. Restricted access increases assembly time and can make consistent torque application more difficult.

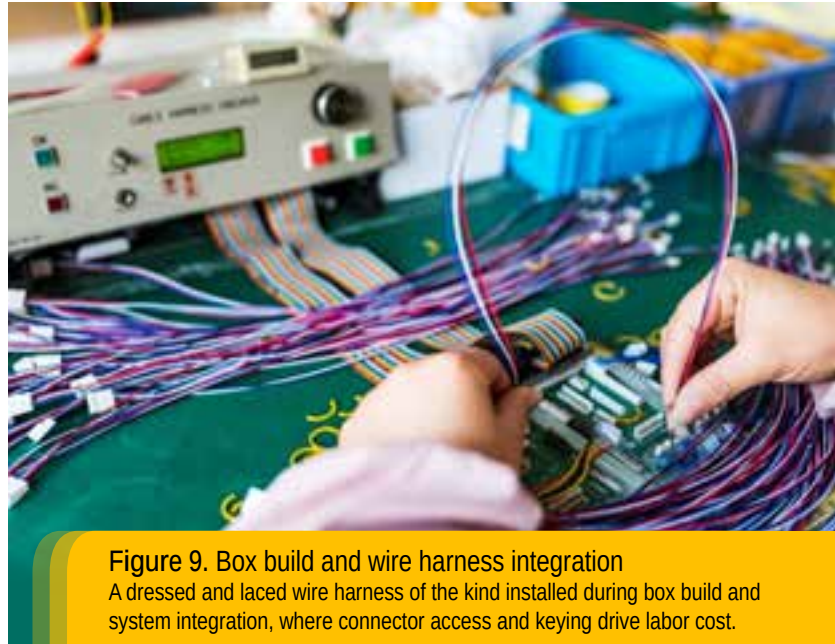


Figure 9. Box build and wire harness integration
A dressed and laced wire harness of the kind installed during box build and system integration, where connector access and keying drive labor cost.

Harness routing should account for appropriate cable length, service loops, bend radius, strain relief, airflow, heat sources, and sharp or moving mechanical features. Harnesses that are too short can stress connectors and terminations, while excessive length can snag, chafe, restrict airflow, or interfere with enclosure assembly and servicing.

Cost Lever Because box build is labor intensive, accessibility, efficient harness routing, and poka-yoke features can reduce assembly time and prevent errors on every unit built. Designing for straightforward, mistake-proof assembly reduces rework, minimizes process variability, and converts directly into lower recurring labor cost.

Across Every Stage

Check 10 — Component Standardization & BOM Health

The final check spans every stage of manufacturing and can significantly influence both the initial quote and long-term production cost. This review evaluates the bill of materials for sourcing risk, lifecycle status, and manufacturability. It looks for opportunities to reduce the number of unique part numbers,

standardize package sizes where practical, avoid components approaching end of life, and identify qualified alternate or multi-source components.

A high number of unique components increases procurement complexity, feeder complexity, setup time, inventory, and minimum-order quantity exposure. Sole-source or end-of-life components increase the risk of shortages, costly substitutions, production delays, and PCB redesigns when replacements are no longer available. Where alternates are specified, they should be verified for electrical, mechanical, thermal, and assembly compatibility rather than assumed to be interchangeable.

BOM quality matters as well. A clean, revision controlled BOM should include complete manufacturer names and part numbers, quantities, reference designators, descriptions, and approved alternates where applicable. Missing or ambiguous information generates engineering queries, slows quoting and procurement, and increases the risk of sourcing and assembly errors.

Cost Lever A standardized, well-controlled BOM reduces procurement risk, component inventory, feeder complexity, setup time, and minimum-order-quantity exposure. Quality alternates improve sourcing flexibility, while complete BOM data accelerates quoting and purchasing by reducing clarification and engineering review. These benefits extend throughout the product lifecycle, helping stabilize cost and reduce the risk of supply-driven production disruptions.

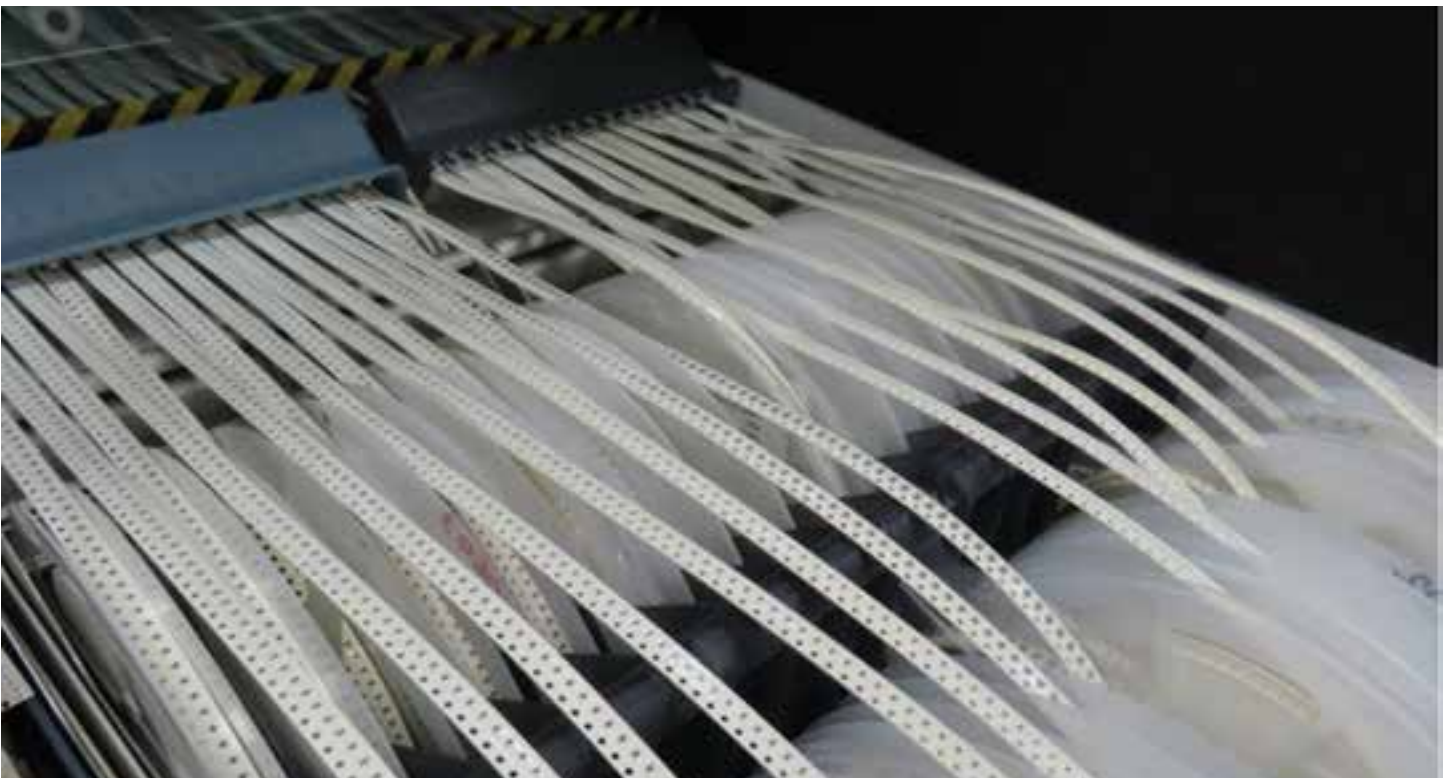


Figure 10. Component standardization and BOM health

Surface-mount components in carrier tape on reels, the form in which parts feed the line; unique part count and sourcing risk are set on the BOM.

OPERATIONALIZING DFM AS A SHARED DISCIPLINE

The ten checks in this paper share a common logic: each identifies a cost or manufacturing risk that is committed early but often discovered and paid for later. DFM moves that discovery into the design and pre-quote window where changes are easier and far less expensive to make. None of these checks is difficult in isolation. The challenge is organizational: they sit at the intersection of engineering, sourcing, and manufacturing, where design decisions, component choices, supply commitments, and production requirements converge.

The most effective way to capture the value of DFM is to involve manufacturing before the design is frozen. A review conducted while the layout, BOM, and manufacturing data are still flexible can turn potential respins, rework, complex tooling, supply disruptions, and recurring labor into relatively simple design changes. Early manufacturing input also gives sourcing a more complete basis for obtaining accurate, comparable quotes.

The goal is not to shift design authority to the manufacturer. It is to give engineering, sourcing, and manufacturing a shared framework for identifying risk and controlling cost before either becomes embedded in the product. The earlier DFM happens, the more options remain, and the less expensive those options are to implement.

REVCO PRODUCTS INC.

Revco Products Inc. is a family-owned electronics manufacturing services (EMS) provider based in Garden Grove, California, with nearly five decades of electronics manufacturing experience. Founded in 1977, Revco provides full-service PCB assembly across surface mount, through-hole, and mixed technologies, along with prototyping, box build and system integration, supply-chain management, and testing.

Every program begins with a Design for Manufacturability (DFM) review to identify cost and manufacturing risks while the design is still easy to change. Revco is ISO 9001 certified and ITAR registered, supporting IPC-A-610 and J-STD-001 workmanship requirements and RoHS-compliant manufacturing for aerospace, defense, medical, automotive, industrial, and commercial applications.

Start with a DFM review

To discuss a current design or an upcoming program, contact Revco Products at (714) 891-6688 or (800) 658-4658, or visit revcoproducts.com. 7221 Acacia Avenue, Garden Grove, CA 92841.

STANDARDS REFERENCED

The checks in this paper refer to the following industry standards. Editions and applicable classes should be confirmed against the current IPC releases and the target program requirements.

Standard	Scope
IPC-2221	Generic standard on printed board design; conductor spacing, clearances, hole and pad sizing.
IPC-7351	Surface mount land patterns and courtyard density levels (Checks 3 and 4).
IPC-7525	Stencil design guidelines; aperture and area-ratios rules (Check 6).
IPC-A-600	Acceptability of bare printed boards; annular ring, plating, mask (Check 1).
IPC-6012	Qualification and performance specification for rigid printed boards.
IPC-A-610	Acceptability of electronic assemblies; defines workmanship Class 1, 2, and 3.
J-STD-001	Requirements for soldered electrical and electronic assemblies; process comparison to IPC-A-610.
IPC-D-356	Netlist format for bare-board electrical test (Checks 3 and 8).
IPC-2581 / ODB++	Intelligent, self-describing design data transfer formats for low-friction handoff (Section 3).
IPC/WHMA-A-620	Requirements and acceptance for cable and wire harness assemblies (Check 9).